IRS FlexRIO OPIF 50MBit/s

Documentation

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1.0	01.07.2020	Christian Bauer	First Draft

CONTENT

IRS FlexRIO OPIF 50MBit/s

1. General

1.1. Purpose of this document

This document describes the optical interface module for Flex-RIO, which contains

- 4 optical transmitters and
- 4 optical receivers.

Both transmitters and receivers are suitable for "Versatile Link" plastic optical fibers at speeds up to 50MBit/s respectively. In the following chapters the hardware and the basic software drivers are highlighted.

1.2. Applicable documents

No	Document	Description
1	AV02-4369EN.pdf	Optical transceiver datasheet (AFBR-1624Z/2624Z)
2	FlexRIO-7953R.pdf	NI FlexRIO FPGA Module Installation Guide and Specifications

1.3. Abbreviations

Abbreviation	Description
FPGA	Field Programmable Gate Array
IO	Input/Output
OPIF	Optical interface
Rx	Receive
Tx	Transmit
VI	Virtual Instrument

2. Hardware

Figure 1: Flex RIO OPIF Module Front View

Figure 2: Flex RIO OPIF Module Side View

2.1. Technical Data of Module

Following table shows the general technical data of the module.

Item	Min	Typ.	Max	Unit
Ambient Temperature	5		60	°C
Supply Voltage (supplied by FlexRIO)	3.135	3.3	3.465	V
Baudrate	0		50	MBit/s

For detailed technical data of transmitters and receivers, refer to AFBR-1624Z/2624Z datasheet.

2.2. AFBR-1624Z Transmitter

Electrical Characteristics

Item	Min	Typical	Max	Unit	Notes
Supply Current (Optical Power ON)		21	31	mA	1
Input Voltage – Low	-0.3		0.8	V	2
Input Voltage – High	2.0		Vcc+0.3	V	2
Data Input Capacitance			7	pF	
Data Input Resistance	2			kΩ	
Propagation Delay			30	ns	

Optical Characteristics

Item	Min	Typical	Max	Unit	Notes
Output optical power (peak), 1 mm POF	-4.5	-2	2	dbm	3
Output optical power (peak), PCS (200 µm)	-16.5	-13	-9	dbm	3
Output optical power (Average), OFF			-50	dbm	
Peak wavelength	630		685	nm	
Rise time (20%–80%)			5	ns	
Fall time (20%–80%)			5	ns	
Pulse width distortion	-3		3	ns	4, 5
Pulse width distortion of first pulse	-5		3	ns	5, 6

Notes

1. For any type of data between DC and 50 Mbd. Typical value 21 mA for PRBS-7 pattern at 25 °C at 5 V and 50 Mbaud.
2. Standard TTL compatible input.
3. Measured with polished connector end face: after 1 meter 1 mm POF, NA = 0.5, or 200 µm PCS, NA = 0.37.
4. Pulse width is measured at 50% threshold using a rising edge trigger tested with PRBS-7 pattern.
5. Electrical input pulse width is determined at 1.5 V and dU/dt between 1 V and 2 V shall not be less than 1 V/ns.
6. The first pulse is shorter as the LED is completely discharged. This helps to mitigate the increase of pulse width of the first pulse of the receiver

2.3. AFBR-2624Z Receiver

Electrical Characteristics

Item	Min	Typical	Max	Unit	Notes
Supply Current		20	30	mA	
Data Output Voltage – Low	-0.3		0.4	V	1, 3
Data Output Voltage – Hig	2.5		VCC+0.3	V	1, 3
Rise Time (10%–90%)			5	ns	2, 3
Fall Time (10%–90%)			5	ns	2, 3
Pulse Width Distortion	-4		4	ns	3, 6, 7, 8, 11
Pulse Width Distortion 1st to 3rd pulse	-5		8	ns	3, 8, 9, 11
Propagation Delay			30	ns	
Max. Initiation time after Power u			15	ms	12

Optical Characteristics

Item	Min	Typical	Max	Unit	Notes
Input Optical Power (Peak), 1 mm POF	-22		2	dBm	3
Input Optical Power (Peak) Off -State, 1 mm POF	-40			dBm	3
Input Optical Power (Peak), PCS (200 µm)	-25		1	dBm	3
Input Optical Power (Peak) Off -State, PCS (200 µm)	-44			dBm	3
Optical Spectrum Range	630		685	nm	

Notes

1. Standard TTL output.
2. Measured with RL = 50 kOhm and CL = 15 pF.
3. Guaranteed only if optical input signal to the receiver is generated by AFBR-16xxZ, with ideal alignment to photo diode using 1mm POF (NA=0.5)
4. –
5. –
6. Optical input signal of 50 MBd, PRBS 27 -1 pattern and 50% duty cycle.

7. Pulse width is measured at 50% threshold using a rising edge trigger and PRBS 27-1 pattern.
8. If data rate is below 1MBd the pulse width distortion would be equal to the pulse width distortion of the 1st to 3rd pulses for higher datarates.
9. The threshold of the 1st pulse of a data sequence is difficult to adjust and therefore the pulse width distortion up to the 3rd pulse is higher than for all other pulses (worst case for the 1st pulse). This strongly depends on the quality of the rising and falling edge of the optical input. The faster the edges the smaller the pulse width variation. Furthermore lower data rates would result in the same issue as all the pulses become 1st pulses.
10. –
11. Because of optical pulse width spreading, the PWD limits have to be increased by +- 0.1 ns for each 10 m fiber length.
12. Starting point is when supply voltage passes ~2.8 V.

3. Software

In the following chapter the example projects are described. The software is developed and tested with LabVIEW 2015 for a NI FlexRIO PXI-7953R Module.

The provided software example has the following folder structure:

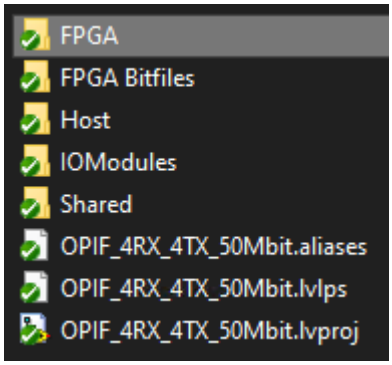

Figure 3: Software Folder Structure

The folder contains the LabVIEW project and the following subfolders

Folder	Content
FPGA	FPGA VIs
FPGA Bitfiles	FPGA Bitfiles
Host	Host (Application) VIs
IOModules	Module Configuration for FlexRIO PXI-795xR series
Shared	Shared VIs (FPGA / Host)

The LabVIEW Example project contains two examples ("Basic Access" and "DMA Access"), which are described in the following sections.

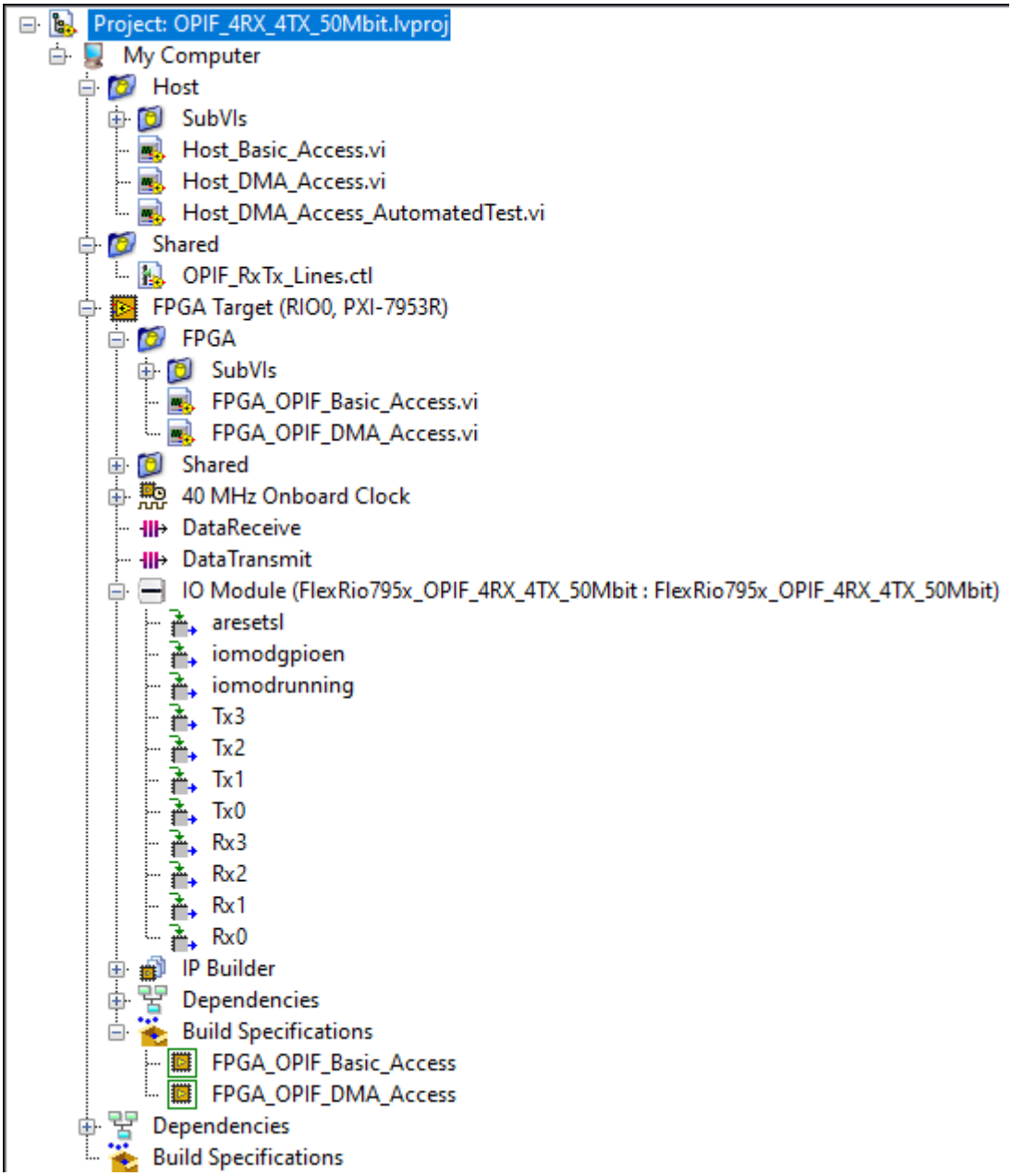

Figure 4: LabVIEW Project Structure

Please note:
The examples are basic examples to show a simple implementation. Implementation details such as error handling oder DMA overflow are not considered in order to keep the example easy to understand and quickly readable.

Please note:
The compilation of the FPGA code might not succeed on Windows 10 as operating system. For more information see https://www.ni.com/de-de/support/documentation/compatibility/17/labview-fpga-module-compatibility-with-windows-10.html
If that's the case, please try to compile on Windows 7 or use the NI Compile Cloud.

3.1. Basic Access Example

As the name indicades, this is a very simple example. In the project there is the FPGA-Top-VI `FPGA_OPIF_Basic_Access.vi` which can be started from the host directly. As an alternative, the corresponding host VI (`Host_Basic_Access.vi`) can be used instead.

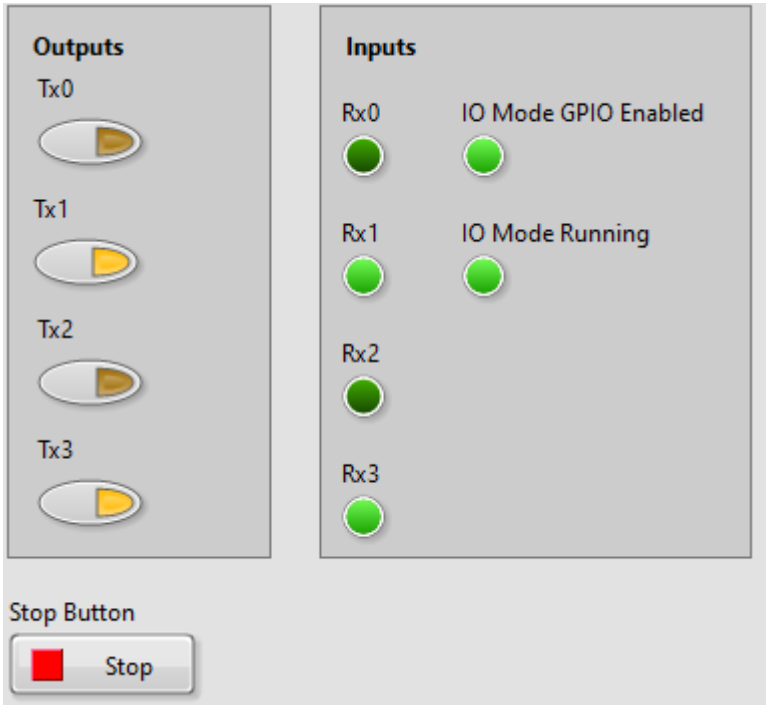

Figure 5: Basic Access: Front Panel Host VI

With the four Tx buttons, the transmitter outputs can be controlled. The four Rx LEDs indicate the state of the receiver inputs. In the figure above, the transmitter outputs are connected to the corresponding receivers.

"IO Mode GPIO Enabled" and "IO Mode Running" indicate that the GPIOs are enabled and the FPGA is running. This is the case, if the vendor and product ID in the EEPROM of the Module fits the IDs in the FPGA Code. If a different module (different product or vendor ID) is insereted, these indicators would be false.

3.2. DMA Access Example

The DMA Access Example is a bit more complex. For this example two OPIFs are in use. The transmitters are connteced to the corresponding receivers (Rx0 - Tx0, Rx1 - Tx1,...). One pair is configured as the data line (Rx/Tx_0 in the figure below), wheras the other pair is the signal line (Rx/Tx_3 in the figure below). The lines are selected in the host Top-VI is `Host_DMA_Access.vi` and must not be the same. The signal line is logic "0" per default. If data is transferred through the data channel, the signal line is "1". This ist the indicator for the receiver, that valid data is transferred.

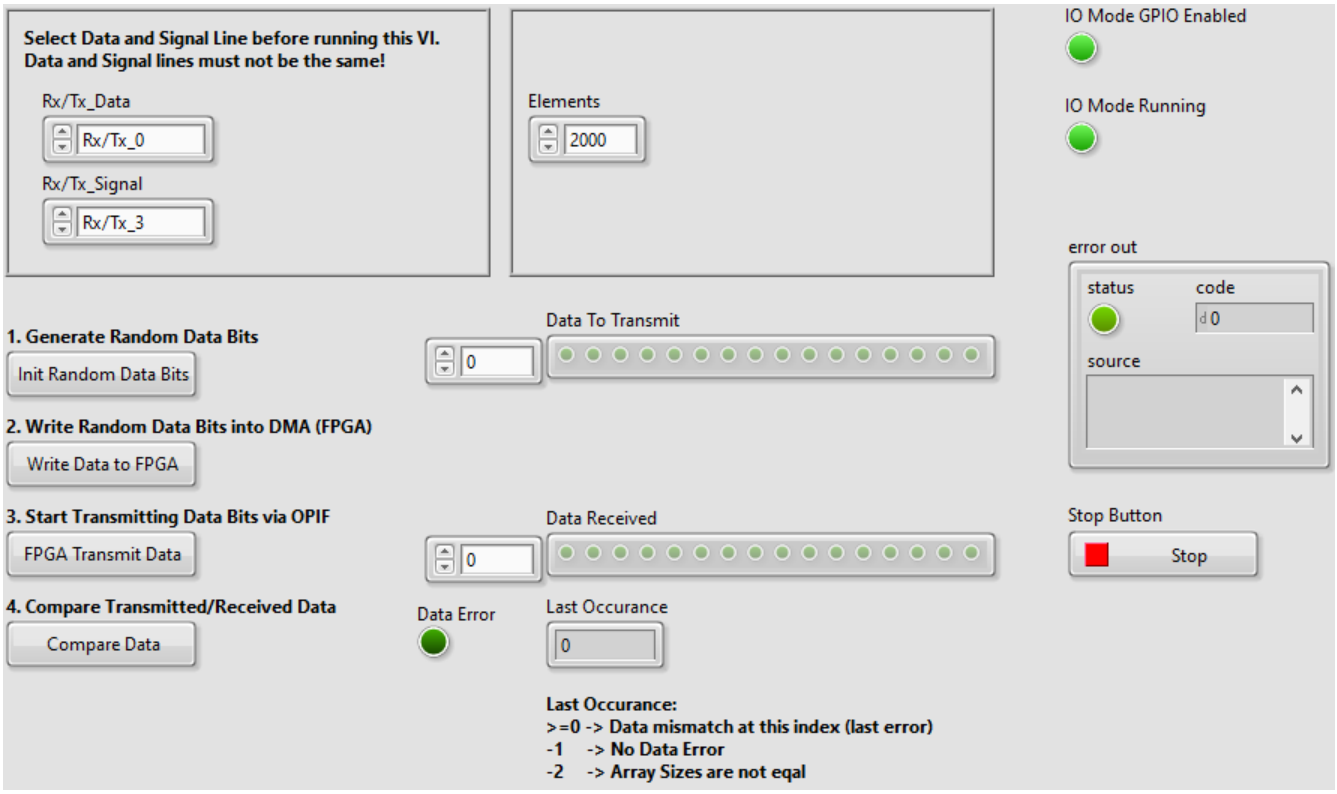

Figure 6: DMA Access: Front Panel Host VI

In order to test the communication, the following steps can be performed:

1. Create a (random) bit-pattern (Length "Elements"-Property, max. 2048!) in the host.
2. Write bit-pattern into the DMA "DataTransmit".
3. Force FPGA to transmit the bit-pattern via OPIF.
    1. FPGA transmits data (50MBit/s) over selected "Rx/Tx_Data" line with a leading "1", while "Rx/Tx_Signal" is high.
    2. FPGA checks the OPIF inputs (200MHz). If the signal line is high, the data gets processed as described below and written into the DMA "DataReceive"
    3. Host reads DMA "DataReceive"
4. Comparison of transmitted and received data.

As the following figure shows, the transmitting loop runs at 50MHz and the receiving loop at 200MHz.

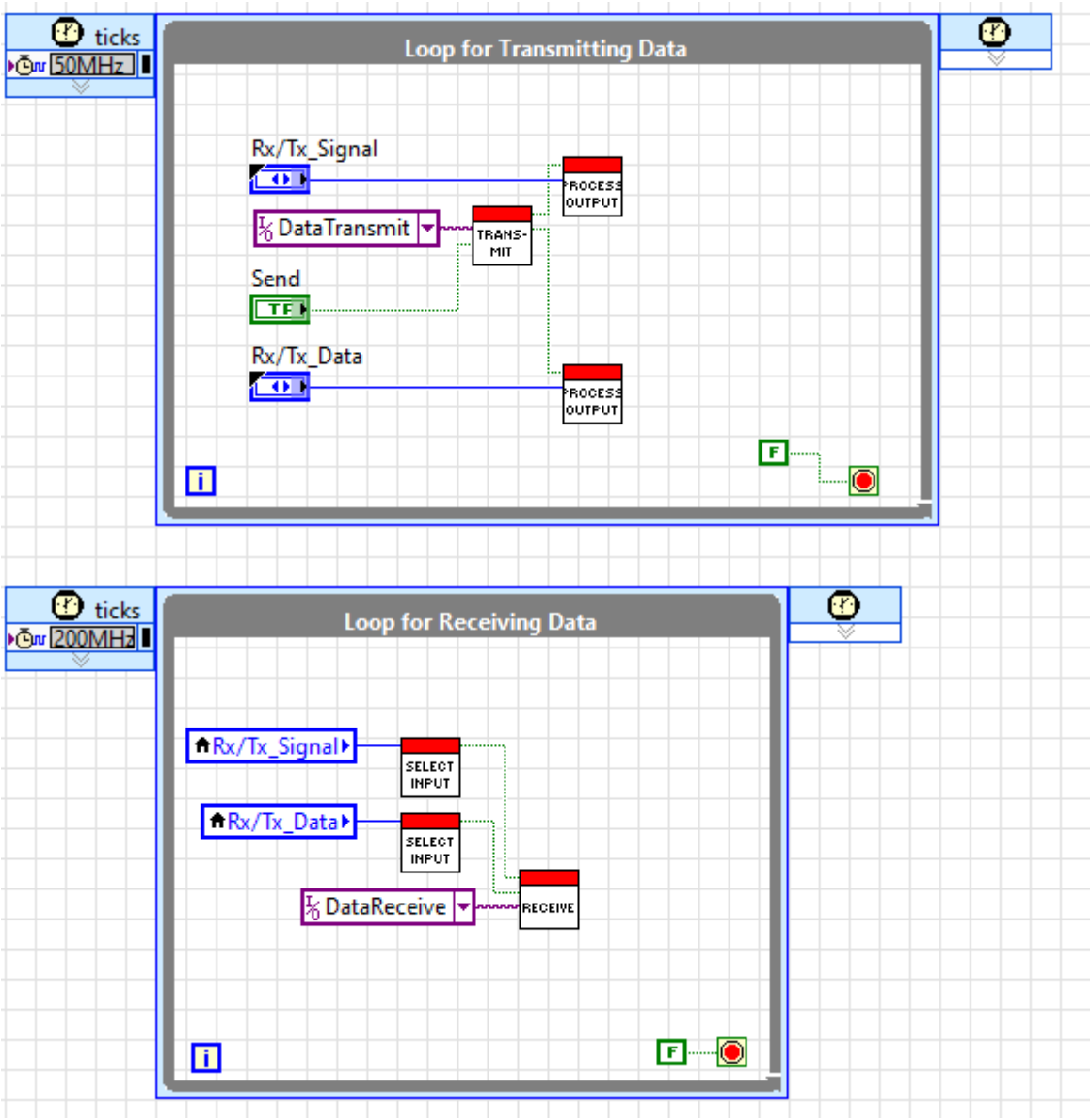

Figure 7: DMA Access: FPGA Top VI - Block Diagram

The FPGA-VI `FPGA_Receive.vi` processes the input data. As mentioned above, the inputs are processed with 200MHz, which is 4 times the frequency of the sender. While the transmitter sends one bit, the receiver receives four. In order to detect a logic "1", the mid two bits must be "1". Also, the first 1 (4) bits will be discarded (see above: first sent bit is 1).

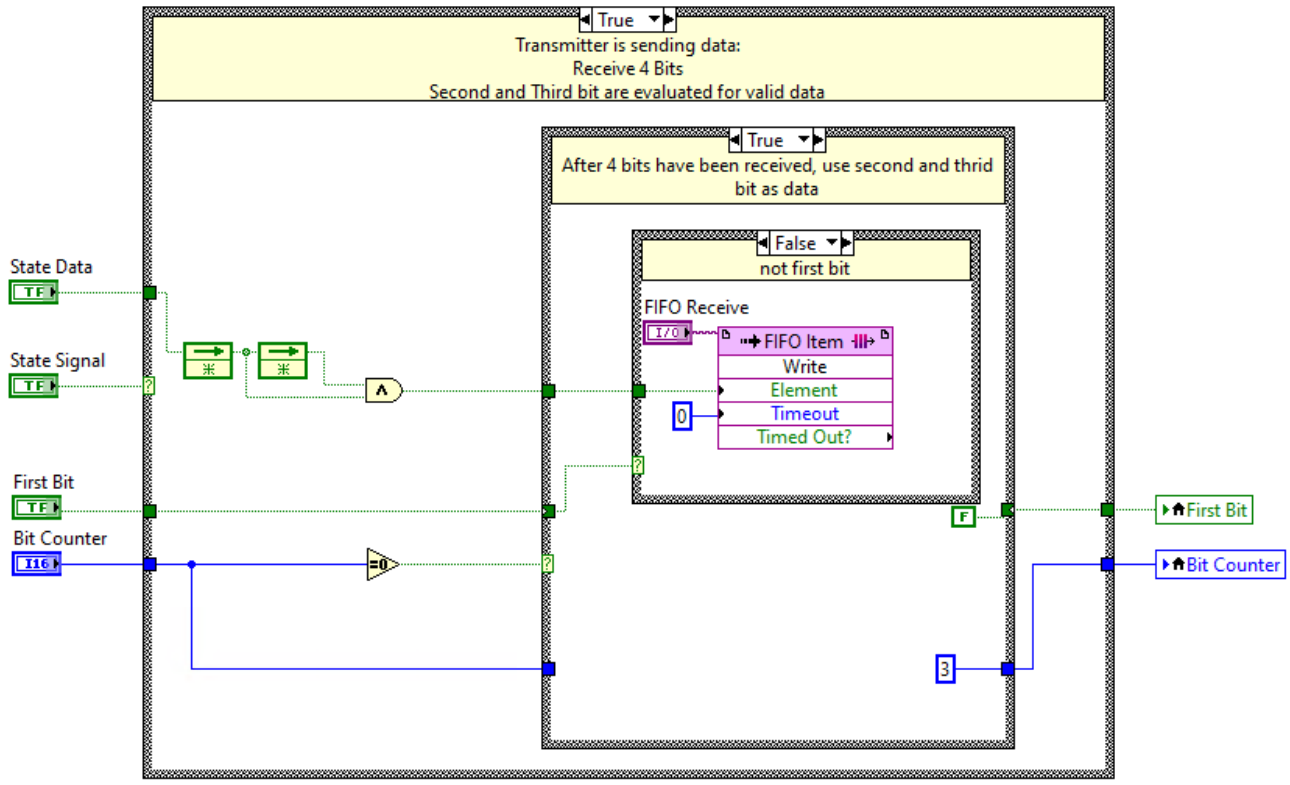

Figure 8: DMA Access: FPGA Receive Block Panel

3.3. How to develop your own software

3.3.1. Requirements

Hardware:

- Development PC
- PXI Chassis
- NI FlexRIO FPGA module
- FlexRIO OPIF Module

Software:

- NI LabVIEW
- NI LabVIEW FPGA Module (incl. Compilation Tools)
- NI-RIO driver or NI FlexRIO driver
- (Optional) LabVIEW Real-Time Module

3.3.2. IO Module Configuration

In order to develop an FPGA application, the correct IO Module configuration needs to be provided to LabVIEW. IRS provides a IO Module Configuration for the NI FlexRIO PXI-795xR series with the example software. The configuration is placed in the subfolder "IOModules".

WARNING!

Different modules such as 797xR have different pinnings!

To access the configuration in LabVIEW, the files need to be placed in the folder `C:\Users\Public\Documents\National Instruments\FlexRIO\IO Modules\` or `C:\Program Files (x86)\National Instruments\Shared\FlexRIO\IO Module\` (recommended; might vary depending on your installation path). We recommend to create a subfolder for the configuration:

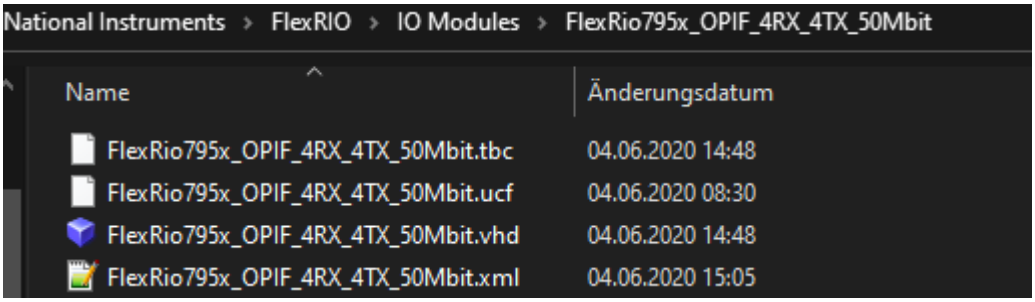

Figure 9: FlexRIO OPIF IO Module Configuration - Subfolder

We recommend to have LabVIEW closed while copying the files.

After placing these files into the (sub-)folder, the module configuration can be accessed through LabVIEW (Properties of "IO Module").

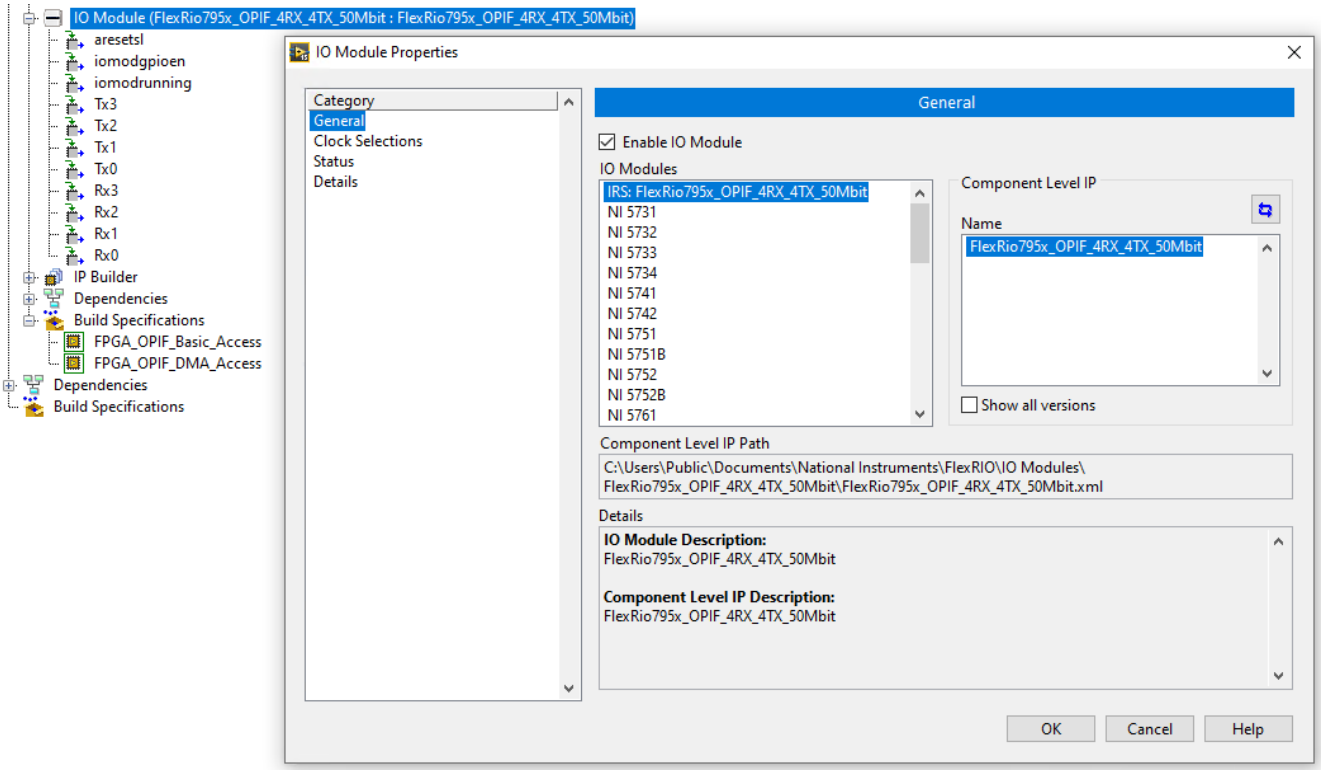

Figure 10: Select FlexRIO OPIF IO Module Configuration

Once the IO module configuration is selected, the receive (Rx) inputs and transmit (Tx) outputs are available in the project.

